CLAIMS

What is claimed is:

1. (Currently amended) A programmable logic device, comprising:

a plurality of function cells, each of the [[a]] function cells [[that]] configured to provide[[s]] a result logic value in response to one or more input logic values and a static or dynamic function vector, each of the function cells having an arithmetic logic circuit that in a first mode is operable to provide the result logic value as a first [[an]] arithmetic combination of the input logic values and in a second mode is operable to provide the result logic value as a ~~logical~~ second arithmetic combination of the input logic values, the first arithmetic combination and the second arithmetic combination determined by the function vector, the first mode and the second mode selected by a global function select signal coupled to at least two of the plurality of function cells ~~arithmetic combination and the logical combination both determined by the function vector~~.

2. (Original) A programmable logic device according to claim 1, wherein the first and second modes are defined by a received arithmetic mode enable signal, the arithmetic logic circuit being operable to determine the defined mode from the received arithmetic mode enable signal.

3. (Currently amended) A programmable logic device according to claim 1, wherein the arithmetic logic circuit further provides a carry output in response to the input logic values, the function vector, the global function select signal, and a carry input.

4. (Currently amended) A programmable logic device according to claim 1, wherein the first arithmetic combination is one of an add, a subtract, an increment, and a decrement operation.

5. (Currently amended) A programmable logic device according to claim [[3]] 1, wherein the second arithmetic combination is one of an add, a subtract, an increment, and a decrement operation.

6. (Canceled)

7. (Currently amended) A programmable logic device according to claim 1, wherein each of the plurality of function cells is operable to receive the function vector from a configuration memory.

8. (Currently amended) A programmable logic device according to claim 1, wherein each of the plurality of function cells is operable to receive the function vector from dynamic configuration signals.

9. (Cancelled)

10. (New) A method for operating a programmable logic device, the method comprising:

receiving one or more input values into a function cell, the function cell included in a plurality of function cells;

receiving a first function vector and a second function vector from a configuration memory into each of the plurality of function cells;

selecting the first function vector or the second function vector based on a global function select signal coupled to at least two of the function cells; and

performing a combination on the input logic values in an arithmetic logic circuit included in the function cell based on the selected function vector.

11. (New) The method of claim 10, wherein the function cell comprises a bit-slice of an arithmetic logic unit.

12 (New) The method of claim 10, further comprising receiving an arithmetic mode enable signal into each of the plurality of function cells, wherein the combination comprises an arithmetic combination or a logical combination based on the selected function vector and the arithmetic mode enable signal.

13. (New) The method of claim 10, wherein performing a combination on the input logic values comprises generating a carry output.

14. (New) The method of claim 10, wherein the combination is one of an add, a subtract, an increment, and a decrement operation.

15. (New) The method of claim 10, wherein selecting the first function vector or the second function vector further comprises:

receiving a dynamic function vector;

receiving a function enable signal; and

enabling the global function select signal based on the function enable signal.

16. (New) A programmable logic device, comprising:

a plurality of function cells configured to receive a first function vector and a second function vector from a configuration memory, receive one or more input values, and receive a global function select signal, each of the plurality of function cells including:

arithmetic logic circuitry configured to perform an arithmetic combination on the input logic values depending on a selected function vector; and

selection circuitry configured to determine the selected function vector from a dynamic function vector, the first function vector and the second function vector based on the global function select signal and a function enable signal, and communicate the selected function vector to the arithmetic logic circuitry.

17. (New) The method of claim 16, wherein the arithmetic logic circuitry is further configured to generate a carry output.

18. (New) The method of claim 16, wherein the arithmetic combination is one of an add, a subtract, an increment, and a decrement operation.